LARGE SIGNAL TRANSISTOR OSCILLATOR DESIGN

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A computer-aided general approach is described for single-transistor oscillator design. The embedding network is built up, step-by-step, to meet all the objectives: spurious free oscillation, output power, efficiency, electronic tuning range and low FM noise.

Introduction

This paper presents a computer-aided general approach for the design of large-signal transistor oscillators. This procedure can be used at any frequency within the active frequency range of the transistor. A network design strategy has been developed to realize an embedding network, which is built up, step-by-step, to meet all the objectives: spurious free oscillation, output power, efficiency, electronic tuning range, and low FM noise.

No previous large signal characterization of the transistor is required. The necessary information is collected during the design procedure, which consists of interleaving steps of measurement and calculation. These steps are computerized. The measurements are performed by a computer operated transmission measuring set (COTMS)[1] and by an HP8542A Automatic Network Analyzer. The measured data are fed directly into an IBM 360 digital computer, which performs the necessary calculations.

Small Signal Analysis

A single transistor oscillator can be represented at any particular frequency by any of the two equivalent circuits of Fig. 1. One of the embedding network elements represents the load, the other two are usually (but not necessarily) lossless. To satisfy the conditions of oscillation, equation

$$Z_L\ (\omega_o) = -Z_{out}\ (\omega_o)$$

or

$$Y_L\ (\omega_o) = -Y_{out}\ (\omega_o)$$

has to be met at the desired frequency of oscillation ω_o. For a given transistor (characterized by its measured small signal two port S parameters) and oscillator topology, a computer program OSC2 calculates and plots oscillator circuit parameters, such as the small signal load impedance or admittance

$$Z_L = \text{RLOAD} + j\text{XLOAD}$$

or

$$Y_L = \text{GLOAD} + j\text{BLOAD},$$

the small signal power gain of the oscillating transistor GAIN, and the generator admittance presented to the transistor by the embedding

$$Y_G = \text{GGEN} + j\text{BGEN}$$

as two variable functions of the feedback reactances X_1 and X_3 or susceptances B_2 and B_3. These "maps" are calculated at a number of frequencies across the active frequency range of the transistor. They give an overall view of the oscillator behavior and can be used to derive constraints for the frequency characteristics of the individual embedding network elements. These constraints are to be satisfied to meet some of the design objectives.

One such "map" RLOAD (X_1,X_3) calculated at 1.9 GHz for an open circuit stable Z oscillator is shown in Fig. 2. The printed numbers give the value of the small signal load resistance. No oscillation is possible in the blank area of the figure.

Fig. 3 shows the necessary frequency characteristics of reactances $X_1(f)$ and $X_3(f)$ to avoid spurious oscillation with this particular transistor. The $X_3[X_1(f)]$ reactance curve projected on the 1.9 GHz RLOAD "map" is shown as curve "a" in Fig. 2. By similarly projecting the $X_3[X_1(f)]$ reactance curve on all RLOAD(X_1,X_3) maps within the active frequency range of the transistor, the possibility of any spurious (out of band) oscillation can be checked by simple inspection.

The other "maps" and the measured noise figure (as a function of the driving generator admittance) of the transistor are used to estimate and to minimize, by making trade-offs with other requirements, the expected FM noise of the oscillator. This step includes calculation of the necessary resonator Q and positioning of operating point f_o on the maps (see Fig. 2).

The two lossless elements of the embedding can be synthesized from the derived constraints. These two ports are then built to permit large signal measurements on the partly-built oscillator.

Large Signal Analysis

The large signal characterization of the transistor is reduced to large signal active one-port measurements: the measurements of the output impedance of the partly-built oscillator at different signal levels and frequencies. The measurements are made semi-automatically by the HP8542A Automatic Network Analyzer, using a newly developed measurement program. A TWT was added to the set to increase the power and an impedance transformer added to avoid oscillation in the circuit under test. The collected data can be plotted as the "Rieke" diagram of the oscillator in a form shown in Fig. 4. Repeated large signal measurements are used to optimize the oscillator efficiency, i.e., to find the best operating point on the small signal "maps." The value of the optimum load can be determined from the "Rieke" diagram directly.

Not only are the number of parameters to be measured reduced by using the partly-built oscillator, but the inherent difficulties in large signal two-port characterization (with S parameters for example) are completely avoided this way. By executing these measurements at a fixed transistor bias, all problems associated with finding the appropriate class of device operation are also avoided, because the transistor changes from Class A operation to B or C automatically with increasing signal level.

Tuning

Electronic tuning of a resonator is analyzed in general terms, the trade-off between loss and tuning range is pointed out.

Experimental Results

An experimental 2 GHz oscillator shown in Fig. 5 was built to check the design procedure. It yielded 230 milliwatt output power at 57 percent dc to RF efficiency in good agreement with the predicted values. The oscillator, when driving an X2 multiplier, could meet the noise objectives for a beat oscillator source[2] in a long haul microwave repeater.

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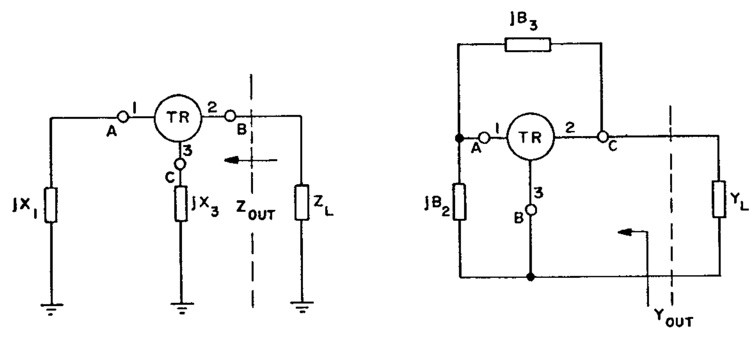

FIG. 1 EQUIVALENT CIRCUIT OF THE Y OR Z TRANSISTOR OSCILLATORS IN CASE OF LOSSLESS "FEEDBACK" ELEMENTS.

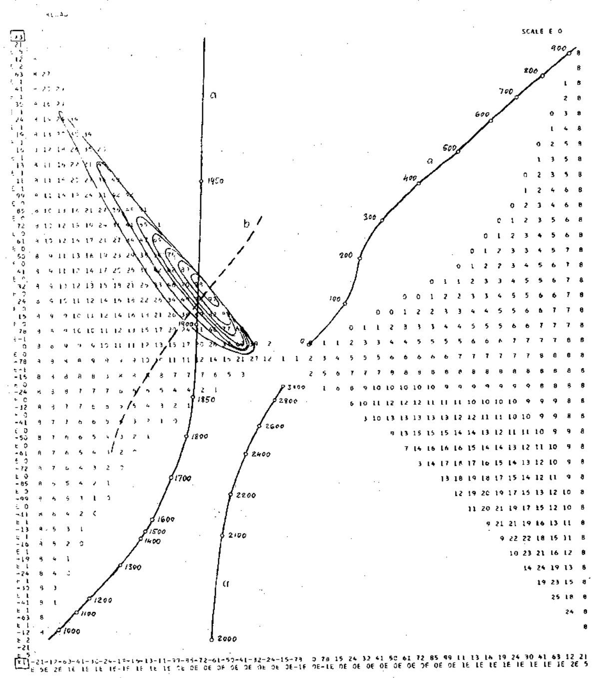

FIG. 2 COMPUTER OUTPUT "RLOAD", CALCULATED AT 1.9 GHz, WITH MEASURED $X_3[X_1(f)]$ CURVE SUPERIMPOSED (CURVE "a").

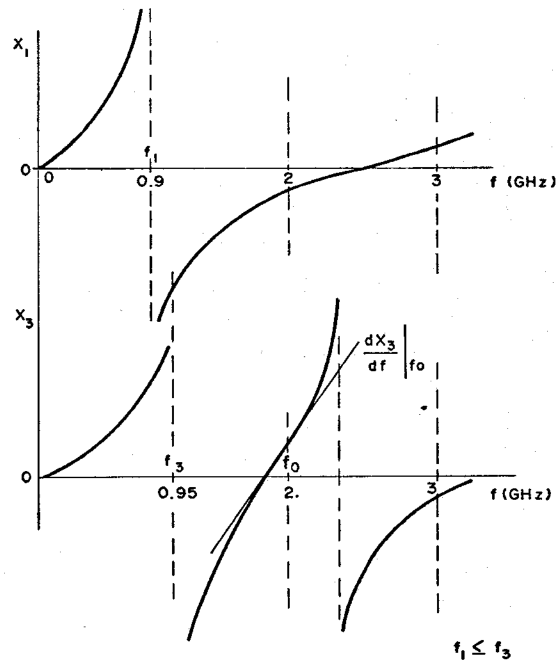

FIG. 3 DESIRED FREQUENCY CHARACTERISTICS OF REACTANCES X_1 AND X_3 IN ORDER TO AVOID SPURIOUS OSCILLATION.

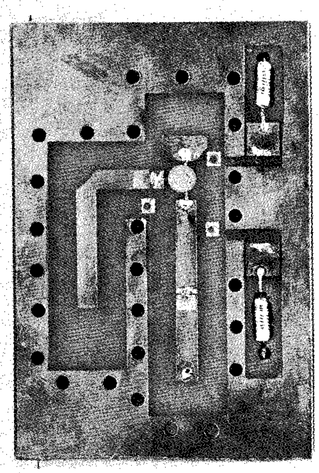

FIG. 5 EXPERIMENTAL 1.9 GHz TRANSISTOR OSCILLATOR IN STRIPLINE.

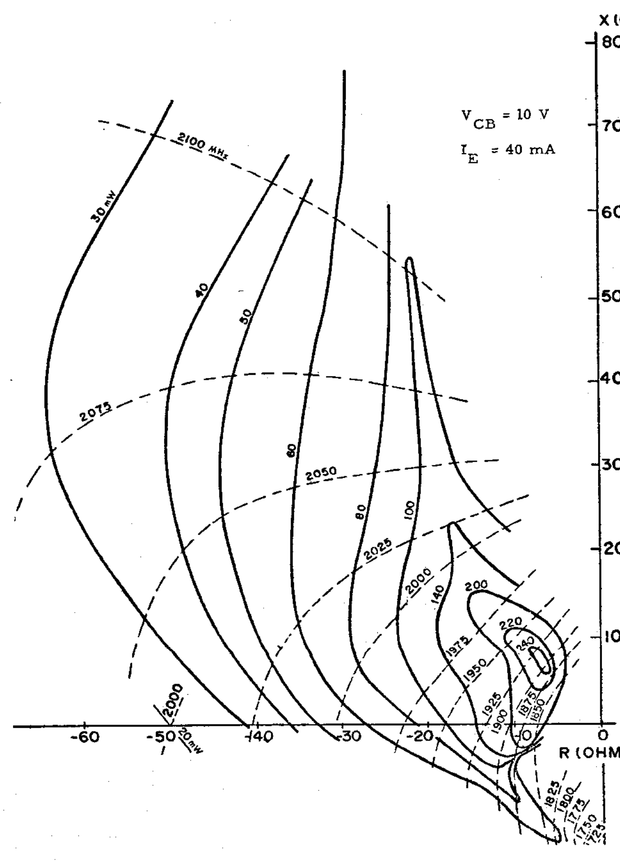

FIG. 4 MEASURED LARGE SIGNAL OUTPUT IMPEDANCE OF AN 1.9 GHz TRANSISTOR OSCILLATOR.